INFORMATION DISCLOSURE STATEMENT BY APPLICANTS PTO FORM 1449	ATTY. DOCKET NO. 2885/98	SERIAL NO. 10/561135 Not yet assigned
	APPLICANT(s) Martin Vorbach et al.	
	FILING DATE Herewith	GROUP Not yet assigned

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EXAMINER INITIAL	PATENT/PUBLICATION NUMBER	PATENT/PUBLICATION DATE	NAME	CLASS	SUBCLASS	FILING DATE
/IA/	*2003/056202	March 20, 2003	Frank et al.			
/IA/	*2002/083308	June 27, 2002	Pereira et al.			
/IA/	*6,282,627	August 28, 2001	Dale et al.			

*Copy of reference is not enclosed because reference is cited and described in Search Report (copy of reference provided by International Searching Authority).

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/IA/	WO 92/01987	February 6, 1992	PCT			X*	

*Copy of reference is not enclosed because reference is cited and described in Search Report (copy of reference provided by International Searching Authority).

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EXAMINER INITIAL	AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.
/IA/	SIEMERS ET AL., "THE >S<PUTER: A NOVEL MICROARCHITECTURE MODEL FOR EXECUTION INSIDE SUPERSCALAR AND VLIW PROCESSORS USING RECONFIGURABLE HARDWARE", 1998, PAGES 169-178, COMPUTER ARCHITECTURE. PROCEEDINGS OF THE AUSTRALASIAN COMPUTER ARCHITECTURE CONFERENCE
/IA/	HAUSER J R ET AL., "GARP: A MIPS PROCESSOR WITH A RECONFIGURABLE COPROCESSOR", APRIL 16, 1997, PAGES 12-21 FIELD-PROGRAMMABLE CUSTOM COMPUTING MACHINES, PROCEEDINGS., THE 5TH ANNUAL IEEE SYMPOSIUM ON NAPA VALLEY, CA, USA
/IA/	WITTIG R D ET AL. "ONECHIP: AN FPGA PROCESSOR WITH RECONFIGURABLE LOGIC" APRIL 17, 1996, PAGES 126-135, FPGAS FOR CUSTOM COMPUTER MACHINES, 1996. PROCEEDINGS. IEEE SYMPOSIUM ON NAPA VALLEY, CA, LOA ALAMITOS, CA USA, IEEE COMPUT. SOC., US
/IA/	KASTRUP B, "AUTOMATIC HARDWARE SYNTHESIS FOR A HYBRID RECONFIGURABLE CPU FEATURING PHILIPS CPLDS", 1998, PAGES 5-10, PROCEEDINGS OF THE PACT WORKSHOP ON RECONFIGURABLE COMPUTING, XX, XX
/IA/	RAZDAN R ET AL., "A HIGH-PERFORMANCE MICROARCHITECTURE WITH HARDWARE PROGRAMMABLE FUNCTIONAL UNITS," NOVEMBER 30, 1994, PAGES 172-180, PROCEEDINGS OF THE ANNUAL INTERNATIONAL SYMPOSIUM ON MICROARCHITECTURE, XX, XX

EXAMINER	/Idriss Alrobaye/	DATE CONSIDERED	11/01/2007

EXAMINER: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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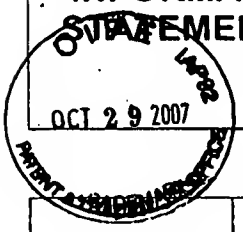

Attorney Docket No.	Serial No.
2885/98	10/561,135
Applicant(s)	
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Filing Date	Group Art Unit
April 25, 2006	2183

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/IA/	RE34363	August 31, 1993	Freeman			
/IA/	2,067,477	January 12, 1937	J.B. Cooper			
	3,242,998	March 29, 1966	C.H. Gubbins			
	3,681,578	August 1, 1972	Stevens			
	3,757,608	September 11, 1973	Willner			
	3,855,577	December 17, 1974	Vandierendonck			
	4,233,667	November 11, 1980	Devine et al.			
	4,489,857	February 6, 1986	Agrawal et al.			
	4,498,134	February 5, 1985	Hansen et al.			
	4,498,172	February 5, 1985	Bhavsar			
	4,566,102	January 21, 1986	Hefner			
	4,591,979	May 27, 1986	Iwashita			
	4,663,706	May 5, 1987	James et al.			
	4,682,284	July 21, 1987	Schrofer			
	4,706,216	November 10, 1987	Carter			
	4,720,778	January, 1998	Hansen et al.			
	4,720,780	January 19, 1988	Dolecek			
	4,739,474	April 19, 1988	Holsztynski			
	4,761,755	August 2, 1988	Ardini et al.			
	4,811,214	March 7, 1989	Nosenchuck et al.			
	4,852,043	July 25, 1989	Guest			
	4,852,048	July 25, 1989	Morton			
	4,860,201	August 22, 1989	Miranker et al.			
	4,870, 302	September 26, 1989	Freeman			
	4,891,810	January 2, 1990	de Corlieu et al.			
	4,901,268	February 13, 1990	Judd			
	4,910,665	March 20, 1990	Mattheyses et al.			
	4,967,340	October 30, 1990	Dawes			
	5,014,193	May 7, 1991	Garner et al.			
	5,015,884	May 14, 1991	Agrawal et al.			
	5,021,947	June 4, 1991	Campbell et al.			
	5,023,775	June 11, 1991	Poret			
	5,043,978	August 27, 1991	Nagler et al.			
	5,047,924	September 10, 1991	Matsubara et al.			
	5,065,308	November 12, 1991	Evans			
	5,072,178	December 10, 1991	Matsumoto			
/IA/	5,081,375	January 14, 1992	Pickett et al.			
/IA/	5,109,503	April 28, 1992	Cruickshank et al.			

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EXAMINER'S INITIALS	PATENT/ PUBLICATION NUMBER	PATENT/PUBLICATION DATE	NAME	CLASS	SUBCLASS	FILING DATE
/IA/	5,113,498	May 12, 1992	Evan et al.			
/IA/	5,115,510	May 19, 1992	Okamoto et al.			
	5,123,109	June 16, 1992	Hillis			
	5,125,801	June 30, 1992	Nabity et al.			
	5,128,559	July 7, 1992	Steele			
	5,142,469	August 25, 1992	Weisenborn			
	5,144,166	September 1, 1992	Camarota et al.			
	5,193,202	March 9, 1993	Lee et al.			
	5,203,005	April 13, 1993	Horst			
	5,204,935	April 20, 1993	Mihara et al.			
	5,208,491	May 4, 1993	Ebeling et al.			
	5,226,122	July 6, 1993	Thayer et al.			
	5,233,539	August 3, 1993	Agrawal et al.			
	5,247,689	September 21, 1993	Ewert			
	5,274,593	December 28, 1993	Proebsting			
	5,287,472	February 15, 1994	Horst			
	5,294,119	March 15, 1994	Vincent et al.			
	5,301,284	April 5, 1994	Estes et al.			
	5,301,344	April 5, 1994	Kolchinsky			
	5,303,172	April 12, 1994	Magar et al.			
	5,311,079	May 10, 1994	Ditlow et al.			
	5,336,950	August 9, 1994	Popli et al.			
	5,347,639	September 13, 1994	Rechtschaffen et al.			
	5,349,193	September 20, 1994	Mott et al.			
	5,353,432	October 4, 1994	Richek et al.			
	5,361,373	November 1, 1994	Gilson			
	5,379,444	January 3, 1995	Mumme			
	5,392,437	February 21, 1995	Matter et al.			
	5,410,723	April 25, 1995	Schmidt et al.			
	5,418,952	May 23, 1995	Morley et al.			
	5,421,019	May 30, 1995	Holsztynski et al.			
	5,422,823	June 6, 1995	Agrawal et al.			
	5,425,036	June 13, 1995	Liu et al.			
	5,426,378	June 20, 1995	Ong			
	5,428,526	June 27, 1995	Flood et al.			
	5,430,687	July 4, 1995	Hung et al.			
	5,440,245	August 8, 1995	Galbraith et al.			
/IA/	5,440,538	August 15, 1995	Olsen et al.			
/IA/	5,442,790	August 15, 1995	Nosenchuck			

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EXAMINER'S INITIALS	PATENT/ PUBLICATION NUMBER	PATENT/PUBLICATION DATE	NAME	CLASS	SUBCLASS	FILING DATE
/IA/	5,444,394	August 22, 1995	Watson et al.			
/IA/	5,448,186	September 5, 1995	Kawata			
	5,455,525	October 3, 1995	Hn et al.			
	5,457,644	October 10, 1995	McCollum			
	5,465,375	November 7, 1995	Thepaut et al.			
	5,473,266	December 5, 1995	Ahanin et al.			
	5,473,267	December 5, 1995	Stansfield			
	5,475,583	December 12, 1995	Bock et al.			
	5,475,803	December 12, 1995	Stearns et al.			
	5,475,856	December 12, 1995	Kogge			
	5,483,620	January 9, 1996	Pechanek et al.			
	5,485,103	January 16, 1996	Pedersen et al.			
	5,485,104	January 16, 1996	Agrawal et al.			
	5,489,857	February 6, 1996	Agrawal et al.			
	5,491,353	February 13, 1996	Kean			
	5,493,239	February 20, 1996	Zlotnick			
	5,497,498	March 5, 1996	Taylor			
	5,506,998	April 9, 1996	Kato et al.			
	5,510,730	April 23, 1996	El Gamal et al.			
	5,511,173	April 23, 1996	Yamaura et al.			
	5,513,366	April 30, 1996	Agarwal et al.			
	5,521,837	May 28, 1996	Frankle et al.			
	5,522,083	May 28, 1996	Gove et al.			
	5,530,873	June 25, 1996	Takano			
	5,530,946	June 25, 1996	Bouvier et al.			
	5,532,693	July 2, 1996	Winters et al.			
	5,532,957	July 2, 1996	Malhi			
	5,535,406	July 9, 1996	Kolchinsky			
	5,537,057	July 16, 1996	Leong et al.			
	5,537,601	July 16, 1996	Kimura et al.			
	5,541,530	July 30, 1996	Cliff et al.			
	5,544,336	August 6, 1996	Kato et al.			
	5,548,773	August 20, 1996	Kemeny et al.			
	5,555,434	September 10, 1996	Carlstedt			
	5,559,450	September 24, 1996	Ngai et al.			
	5,561,738	October 1, 1996	Kinerk et al.			
	5,570,040	October 29, 1996	Lytle et al.			
/IA/	5,574,930	November 12, 1996	Halverson Jr. et al.			
/IA/	5,583,450	December 10, 1996	Trimberger et al.			

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EXAMINER'S INITIALS	PATENT/ PUBLICATION NUMBER	PATENT/PUBLICATION DATE	NAME	CLASS	SUBCLASS	FILING DATE
/IA/	5,586,044	December 17, 1996	Agrawal et al.			
/IA/	5,587,921	December 24, 1996	Agrawal et al.			
	5,588,152	December 24, 1996	Dapp et al.			
	5,590,345	December 31, 1996	Barker et al.			
	5,590,348	December 31, 1996	Phillips et al.			
	5,596,742	January 21, 1997	Agarwal et al.			
	5,600,265	February 4, 1997	El Gamal Abbas et al.			
	5,600,845	February 4, 1997	Gilson			
	5,611,049	March 11, 1997	Pitts			
	5,617,547	April 1, 1997	Feeney et al.			
	5,625,806	April 29, 1997	Kromer			
	5,634,131	May 27, 1997	Matter et al.			
	5,649,176	July 15, 1997	Selvidge et al.			
	5,649,179	July 15, 1997	Steenstra et al.			
	5,652,894	July 29, 1997	Hu et al.			
	5,655,069	August 5, 1997	Ogawara et al.			
	5,655,124	August 5, 1997	Lin			
	5,657,330	August 12, 1997	Matsumoto			
	5,659,797	August 19, 1997	Zandveld et al.			
	5,675,743	October 7, 1997	Mavity			
	5,680,583	October 21, 1997	Kuijsten			
	5,713,037	January 27, 1998	Wilkinson et al.			
	5,717,943	February 10, 1998	Barker et al.			
	5,732,209	March 24, 1998	Vigil et al.			
	5,734,921	March 31, 1998	Dapp et al.			
	5,737,516	April 1998	Circello et al.			
	5,742,180	April 21, 1998	Detton et al.			
	5,748,872	May 5, 1998	Norman			
	5,754,827	May 19, 1998	Barbier et al.			
	5,754,871	May 19, 1998	Wilkinson et al.			
	5,760,602	June 2, 1998	Tan			
	5,761,484	June 2, 1998	Agarwal et al.			
	5,773,994	June 30, 1998	Jones			
	5,778,439	July 7, 1998	Timberger et al.			
	5,784,636	July 21, 1998	Rupp			
	5,794,059	August 11, 1998	Barker et al.			
	5,794,062	August 11, 1998	Baxter			
/IA/	5,801,715	September 1, 1998	Norman			
/IA/	5,802,290	September 1, 1998	Casselman			

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EXAMINER'S INITIALS	PATENT/ PUBLICATION NUMBER	PATENT/PUBLICATION DATE	NAME	CLASS	SUBCLASS	FILING DATE
/IA/	5,828,229	October 27, 1998	Cliff et al.			
/IA/	5,828,858	October 27, 1998	Athanas et al.			
	5,838,165	November 17, 1998	Chatter			
	5,841,973	November 1998	Cooke et al.			
	5,844,888	December 1, 1998	Narjiyka			
	5,848,238	December 8, 1998	Shimomura et al.			
	5,854,918	December 29, 1998	Baxter			
	5,859,544	January 12, 1999	Norman			
	5,865,239	February 2, 1999	Carr			
	5,867,691	February 2, 1999	Shiraishi			
	5,867,723	February 2, 1999	Peters et al.			
	5,884,075	March 16, 1999	Hester et al.			
	5,887,162	March 23, 1999	Williams et al.			
	5,887,165	March 23, 1999	Martel et al.			
	5,889,982	March 30, 1999	Rodgers et al.			
	5,892,370	April 6, 1999	Eaton et al.			
	5,892,961	April 6, 1999	Trimberger			
	5,892,962	April 6, 1999	Cloutier			
	5,901,279	May 4, 1999	Davis III			
	5,915,123	June 22, 1999	Mirsky et al.			
	5,924,119	July 13, 1999	Sindhu et al.			
	5,926,638	July 1999	Inoue, Masaharu			
	5,927,423	July 27, 1999	Wada et al.			
	5,933,642	August 3, 1999	Baxter et al.			
	5,936,424	April 10, 1999	Young et al.			
	5,943,242	August 24, 1999	Vorbach et al.			
	5,956,518	September 21, 1999	DeHon et al.			
	5,960,200	September 1999	Eager et al.			
	5,966,534	October 12, 1999	Cooke et al.			
	5,996,083	November 30, 1999	Gupta et al.			
	5,970,254	October 19, 1999	Cooke et al.			
	5,978,260	November 2, 1999	Trimberger et al.			
	5,996,083	November 30, 1999	Gupta et al.			
	6,003,143	December 1999	Kim et al.			
	6,011,407	January 4, 2000	New			
	6,014,509	January 11, 2000	Furtek et al.			
	6,020,758	February 1, 2000	Patel et al.			
/IA/	6,021,490	February 1, 2000	Vorbach et al.			
/IA/	6,023,564	February 8, 2000	Trimberger			

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/IA/	6,023,742	February 8, 2000	Ebeling et al.			
/IA/	6,034,538	March 7, 2000	Abramovici			
	6,038,650	March 14, 2000	Vorbach et al.			
	6,038,656	March 14, 2000	Cummings et al.			
	6,047,115	April 4, 2000	Mohan et al.			
	6,049,222	April 11, 2000	Lawman			
	6,052,773	April 18, 2000	DeHon et al.			
	6,054,873	April 25, 2000	Laramie			
	6,058,469	May 2, 2000	Baxter			
	6,081,903	June 27, 2000	Vorbach et al.			
	6,085,317	July 4, 2000	Smith			
	6,086,628	July 11, 2000	Dave et al.			
	6,088,795	July 11, 2000	Vorbach et al.			
	6,092,174	July 18, 2000	Roussakov			
	6,105,105	August 15, 2000	Trimberger et al.			
	6,108,760	August 22, 2000	Mirsky et al.			
	6,119,181	September 12, 2000	Vorbach et al.			
	6,122,719	September 19, 2000	Mirsky et al.			
	6,125,408	September 26, 2000	McGee et al.			
	6,127,908	October 3, 2000	Bozler et al.			
	6,150,837	November 21, 2000	Beal et al.			
	6,150,839	November 21, 2000	New et al.			
	6,170,051	January 2001	Dowling, Eric M.			
	6,172,520	January 9, 2001	Lawman et al.			
	6,173,434	January 9, 2001	Wirthlin et al.			
	6,202,182	March 13, 2001	Abramovici et al.			
	6,211,697	April 2001	Lien et al.			
	6,212,650	April 2001	Guccione, Steven A.			
	6,219,833	April 17, 2001	Solomon et al.			
	6,230,307	May 8, 2001	Davis et al.			
	6,240,502	May 29, 2001	Panwar et al.			
	6,243,808	June 5, 2001	Wang			
	6,260,179	July 10, 2001	Ohsawa et al.			
	6,263,430	July 17, 2001	Trimberger et al.			
	6,279,077	August 21, 2001	Nasserbakht et al.			
	6,282,627	August 28, 2001	Wong et al.			
	6,282,701	August 2001	Wygodny et al.			
/IA/	6,286,134	September 2001	Click, Jr. et al.			
/IA/	6,288,566	September 11, 2001	Hanrahan et al.			

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/IA/	6,289,440	September 11, 2001	Casselman			
/IA/	6,298,472	October 2, 2001	Phillips et al.			
	6,301,706	October 2001	Maslennikov et al.			
	6,311,200	October 30, 2001	Hanrahan et al.			
	6,321,366	November 20, 2001	Tseng et al.			
	6,321,373	November 20, 2001	Ekanadham et al.			
	6,338,106	January 8, 2002	Vorbach et al.			
	6,341,318	January 22, 2002	Dakhil			
	6,347,346	February 12, 2002	Taylor			
	6,349,346	February 19, 2002	Hanrahan et al.			
	6,370,596	April 9, 2002	Dakhil			
	6,378,068	April 23, 2002	Fnster et al.			
	6,389,379	May 14, 2002	Lin et al.			
	6,389,579	May 14, 2002	Phillips et al.			
	6,392,912	May 21, 2002	Hanrahan et al.			
	6,398,383	June 2002	Huang, Yu-Hwei			
	6,404,224	June 11, 2002	Azegami et al.			
	6,405,299	June 11, 2002	Vorbach et al.			
	6,421,809	July 2002	Wuytaek et al.			
	6,421,917	July 16, 2002	Mohan			
	6,425,054	July 23, 2002	Nguyen			
	6,425,068	July 23, 2002	Vorbach			
	6,434,695	August 2002	Esfahani et al.			
	6,434,699	August 13, 2002	Jones et al.			
	6,437,441	August 2002	Yamamoto			
	6,457,116	September 24, 2002	Mursdy et al.			
	6,477,643	November 5, 2002	Vorbach et al.			
	6,480,937	November 12, 2002	Vorbach et al.			
	6,480,954	November 12, 2002	Trimberger et al.			
	6,490,695	December 2002	Zagorski et al.			
	6,496,971	December 2002	Lesea et al.			
	6,504,398	January 2003	Lien et al.			
	6,513,077	January 28, 2003	Vorbach et al.			
	6,519,674	February 11, 2003	Lam et al.			
	6,526,520	February 25, 2003	Vorbach et al.			
/IA/	6,538,468	March 25, 2003	Moore			
/IA/	6,539,477	March 25, 2003	Seawright			

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/IA/	6,542,844	April 2003	Hanna, Stephen Dale			
/IA/	6,542,998	April 1, 2003	Vorbach			
	6,571,381	May 27, 2003	Vorbach et al.			
	6,587,939	July 1, 2003	Takano			
	6,657,457	December 2, 2003	Hanrahan et al.			
	6,687,788	February 3, 2004	Vorbach et al.			
	6,697,979	February 24, 2003	Vorbach et al.			
	6,704,816	March 2004	Burke, David			
	6,717,436	April 2004	Kress et al.			
	6,721,830	April 2004	Vorbach et al.			
	6,728,871	April 27, 2004	Vorbach et al.			
	6,757,847	June 2004	Farkash et al.			
	6,785,826	August 31, 2004	Durham et al.			
	6,961,924	November 2005	Bates et al.			
	2001/0010074	July 26, 2001	Nishihara et al.			
	2003/0056085	March 2, 2003	Vorbach			
	2002/0038414	March 28, 2002	Taylor			
	2002/0045952	April 18, 2002	Blemel			
	2002/0143505	October 3, 2002	Drusinsky			
	2002/0144229	October 3, 2002	Hanrahan			
	2002/0165886	November 7, 2002	Lam			
	2003/0014743	January 16, 2003	Cooke et al.			
	2003/0046607	March 6, 2003	Vorbach			
	2003/0052711	March 20, 2003	Taylor			
/IA/	2003/0055861	March 20, 2003	Lai et al.			
/IA/	2003/0056091	March 20, 2003	Greenberg			
/IA/	2003/0056202	March 20, 2003	Vorbach			
/IA/	2003/0093662	May 15, 2003	Vorbach et al.			
/IA/	2003/0097513	May 22, 2003	Vorbach et al.			
/IA/	2003/0123579	July 3, 2003	Safavi et al.			
/IA/	2003/0135686	July 17, 2003	Vorbach et al.			
/IA/	2003/0192032	October 2003	Andrade et al.			
/IA/	2004/0015899	January 22, 2004	May et al.			
/IA/	2004/0025005	February 5, 2004	Vorbach et al.			
/IA/	2004/0168099	August 26, 2004	Vorbach et al.			
/IA/	2004/1099688	October 2004	Vorbach et al.			

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EXAMINER'S INITIALS	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
						YES	NO
/IA/	0 208 457	January 14, 1987	EPO				
/IA/	0 221 360	May 13, 1987	EPO				
/IA/	0 428 327	May 22, 1991	EPO				
/IA/	0 463 721	January 2, 1992	EPO				
/IA/	0 477 809	April 1, 1992	EPO				
/IA/	0 485 690	May 20, 1992	EPO				
/IA/	0 497 029	August 5, 1992	EPO				
/IA/	0 539 595	May 5, 1993	EPO				
/IA/	0 628 917	December 14, 1994	EPO				
/IA/	0 678 985	October 25, 1995	EPO				
/IA/	0 686 915	December 13, 1995	EPO				
/IA/	0 707 269	April 17, 1996	EPO				
/IA/	0 726 532	August 14, 1996	EPO				
/IA/	0 735 685	October 2, 1996	EPO				
/IA/	0 748 051	December 11, 1996	EPO				
/IA/	0 835 685	October 2, 1996	EPO				
/IA/	0 926 594	June 30, 1999	EPO				
/IA/	1 102 674	May 30, 2001	EPO				
/IA/	1 146 432	October 17, 2001	EPO				
/IA/	42 21 278	January 5, 1994	Germany			Abstract	
/IA/	38 55 673	November 20, 1996	Germany			Abstract	
/IA/	100 28 397	December 20, 2001	Germany			Abstract	
/IA/	100 36 627	February 14, 2002	Germany			Abstract	
/IA/	101 29 237	April 18, 2002	Germany			Abstract	
/IA/	102 04 044	August 14, 2003	Germany			Abstract	
/IA/	196 51 075	June 10, 1998	Germany			Abstract	
/IA/	196 54 593	July 2, 1998	Germany			Abstract	
/IA/	196 54 595	July 2, 1998	Germany			Abstract	
/IA/	196 54 846	July 9, 1998	Germany			Abstract	
/IA/	197 04 044	August 13, 1998	Germany			Abstract	
/IA/	197 04 728	August 13, 1998	Germany			Abstract	
/IA/	197 04 742	September 24, 1998	Germany			Abstract	
/IA/	198 07 872	August 26, 1999	Germany			Abstract	
/IA/	198 61 088	February 10, 2000	Germany			Abstract	
/IA/	199 26 538	December 14, 2000	Germany			Abstract	
/IA/	WO90/04835	May 3, 1990	PCT				
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						YES	NO
/IA/	WO93/11503	June 10, 1993	PCT				
/IA/	WO94/06077	March 17, 1994	PCT				
/IA/	WO94/08399	April 14, 1994	PCT				
/IA/	WO95/00161	January 5, 1995	PCT				
/IA/	WO95/26001	September 28, 1995	PCT				
/IA/	WO98/26356	June 18, 1998	PCT				
/IA/	WO98/28697	July 2, 1998	PCT				
/IA/	WO98/29952	July 9, 1998	PCT				
/IA/	WO98/31102	July 16, 1998	PCT				
/IA/	WO98/35299	August 13, 1998	PCT				
/IA/	WO99/00731	January 7, 1999	PCT				
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/IA/	WO99/12111	March 11, 1999	PCT				
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/IA/	WO99/40522	August 12, 1999	PCT				
/IA/	WO99/44147	September 2, 1999	PCT				
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/IA/	WO01/55917	August 2, 2001	PCT				
/IA/	WO02/13000	February 14, 2002	PCT				
/IA/	WO02/21010	March 14, 2002	PCT				
/IA/	WO02/29600	April 11, 2002	PCT				
/IA/	WO02/71248	September 12, 2002	PCT				
/IA/	WO02/071249	September 12, 2002	PCT				
/IA/	WO02/103532	December 27, 2002	PCT				
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/IA/	WO03/023616	March 30, 2003	PCT				
/IA/	WO03/032975	April 24, 2003	PCT				
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						YES	NO
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